



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,970	04/13/2004	Hiroyuki Ogawa	AMD-AFO1215	5318

7590 12/23/2005

WAGNER, MURABITO & HAO LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

EXAMINER

HOANG, QUOC DINH

ART UNIT PAPER NUMBER

2818

DATE MAILED: 12/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/823,970

Applicant(s)

OGAWA ET AL. 

Examiner

Quoc D. Hoang

Art Unit

2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 October 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

1. Amendment filed on 10/12/2005 has been entered and made of record as Paper No. 1005. Claims 1-15 are pending in the application.

Applicants' remarks have been considered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4, 6-11, and 13-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Tanaka., (US Pat No. 6,756,675).

Regarding claim 1, Tanaka teaches a semiconductor device comprising:

a pad metal layer 100 having a perimeter area and a center area (col. 6, lines 20-67 and Fig. 1);

a lower metal layer 200 having a plurality of apertures 130a-130i below said center area of said pad metal layer 100, wherein said apertures 130a-130i are arranged into a plurality of rows each row comprising more than one of said apertures and a plurality of columns each column comprising more than one of said apertures(col. 6, lines 20-67 and Figs. 1-2A); and

an interlayer dielectric 150 formed between said pad metal layer 100 and said lower metal layer 200 (col. 6, lines 20-67 and Fig. 1).

Regarding claim 2, Tanaka teaches a plurality of vias 110a-110d formed in said interlayer dielectric 150, wherein said vias electrically couple said pad metal layer 100 and said lower metal layer 200, and wherein said vias are located below said perimeter area of said pad metal layer 100 (col. 6, lines 20-67 and Fig. 1).

Regarding claim 3, Tanaka teaches wherein said vias 110a-110d are filled with tungsten (col. 6, line 55).

Regarding claim 4, Tanaka teaches wherein the vias 110a-110d, 115a-115b, and 117a-117b are positioned in a ring arrangement below the pad metal layer (col. 7, line 15 and Figs. 1 and 2A).

Regarding claim 6, Tanaka teaches the bonding wire 180 is connected to the pad metal 100, but does not teach wherein **a probing process** is performed on said center area of said pad metal layer. Although the Tanaka does not teach wherein a probing process is performed on said center area of said pad metal layer, the present of the process limitations on product claims, which product does not otherwise patentably distinguish over prior art, cannot impart patentability to the product. In re Stephen 145 USPQ 656 (CCPA 1965).

Regarding claim 7, Tanaka teaches the bonding wire 180 is connected to the pad metal 100, but does not teach wherein **a wire-bonding process** is performed on said center area of said pad metal layer. Although the Tanaka does not teach wherein a wire-bonding process is performed on said center area of said pad metal layer, the

Art Unit: 2818

present of the process limitations on product claims, which product does not otherwise patentably distinguish over prior art, cannot impart patentability to the product. In re Stephen 145 USPQ 656 (CCPA 1965).

Regarding claim 8, Tanaka teaches wherein said semiconductor device is an integrated circuit chip (col. 11, line 28).

Regarding claim 9, Tanaka teaches a semiconductor device comprising:

a pad metal layer 100 having a perimeter area and a center area (col. 6, lines 20-67 and Fig. 1);

a lower metal layer 200 having a plurality of apertures 130a-130i below said center area of said pad metal layer 100, wherein said apertures 130a-130i are arranged into a plurality of rows each row comprising more than one of said apertures and a plurality of columns each column comprising more than one of said apertures (col. 6, lines 20-67 and Figs. 1-2A);

an interlayer dielectric 150 formed between said pad metal layer 100 and said lower metal layer 200 (col. 6, lines 20-67 and Fig. 1); and

a plurality of vias 110a-110d formed in said interlayer dielectric 150, wherein said vias electrically couple said pad metal layer 100 and said lower metal layer 200, and wherein said vias are located below said perimeter area of said pad metal layer 100 (col. 6, lines 20-67 and Fig. 1).

Regarding claim 10, Tanaka teaches wherein said vias 110a-110d are filled with tungsten (col. 6, line 55).

Regarding claim 11, Tanaka teaches wherein the vias 110a-110d, 115a-115b, and 117a-117b are positioned in a ring arrangement below the pad metal layer (col. 7, line 15 and Figs.1 and 2A).

Regarding claim 13, Tanaka teaches the bonding wire 180 is connected to the pad metal 100, but does not teach wherein **a probing process** is performed on said center area of said pad metal layer. Although the Tanaka does not teach wherein a probing process is performed on said center area of said pad metal layer, the present of the process limitations on product claims, which product does not otherwise patentably distinguish over prior art, cannot impart patentability to the product. In re Stephen 145 USPQ 656 (CCPA 1965).

Regarding claim 14, Tanaka teaches the bonding wire 180 is connected to the pad metal 100, but does not teach wherein **a wire-bonding process** is performed on said center area of said pad metal layer. Although the Tanaka does not teach wherein a wire-bonding process is performed on said center area of said pad metal layer, the present of the process limitations on product claims, which product does not otherwise patentably distinguish over prior art, cannot impart patentability to the product. In re Stephen 145 USPQ 656 (CCPA 1965).

Regarding claim 15, Tanaka teaches wherein said semiconductor device is an integrated circuit chip (col. 11, line 28).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

Art Unit: 2818

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 5 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka., (US Pat No. 6,756,675) in view of Heim., (US Pat No. 5,248,903).

Regarding claim 5, Tanaka teaches a protect film 240 that covers said perimeter area of said pad metal layer 100 (col. 7, line 45 and Fig. 2B), but fails to teach the protect film is an insulating dielectric layer.

However, Heim teaches the film 218 is an insulating dielectric layer (col. 4, lines 7-9 and Fig. 2A, borophosphosilicate glass). Since Fujiki and Heim are all from the same field of endeavor, the purpose disclosed by Heim would have been recognized in the pertinent art of Fujiki. It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to provide the an insulating dielectric layer on the perimeter area of the pad metal layer in order to provide the contact area on the top surface of the metal pad layer as taught by Heim, column 4, lines 10-20.

Regarding claim 12, Tanaka teaches a protect film 240 that covers said perimeter area of said pad metal layer 100 (col. 7, line 45 and Fig. 2B), but fails to teach the protect film is an insulating dielectric layer.

However, Heim teaches the film 218 is an insulating dielectric layer (col. 4, lines 7-9 and Fig. 2A, borophosphosilicate glass). Since Fujiki and Heim are all from the same field of endeavor, the purpose disclosed by Heim would have been recognized in the pertinent art of Fujiki. It would have been obvious to a person of ordinary skill in the

art at the time of the invention was made to provide the an insulating dielectric layer on the perimeter area of the pad metal layer in order to provide the contact area on the top surface of the metal pad layer as taught by Heim, column 4, lines 10-20.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quoc Hoang whose telephone number is (571) 272-1780. The examiner can normally be reached on Monday-Friday from 8.00 AM to 5.00 PM.

If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone numbers of

Art Unit: 2818

the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Quoc Hoang 
Patent examiner/AU 2818


David Nelms
Supervisory Patent Examiner
Technology Center 2800